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**Replacement claim 2**

- 1        2. The invention as defined in claim 1 wherein other terminal of said active
- 2        inductor is said first power supply terminal.

**Unchanged claim 3**

- 1        3. The invention as defined in claim 1 wherein said MOS transistor also has a
- 2        bulk terminal, said bulk terminal being connected to a second power supply terminal.

**Unchanged claim 4**

- 1        4. The invention as defined in claim 1 wherein MOS transistor is a negative metal
- 2        oxide semiconductor (NMOS) transistor.

**Unchanged claim 5**

- 1        5. The invention as defined in claim 1 wherein MOS transistor is a positive metal
- 2        oxide semiconductor (PMOS) transistor.

**Unchanged claim 6**

- 1        6. The invention as defined in claim 1 wherein said MOS transistor also has a
- 2        bulk terminal, said bulk terminal being connected to a second power supply terminal, and
- 3        wherein said power supply voltage supplied from said first power supply terminal is
- 4        higher than a voltage supplied from said second power supply terminal.

**Unchanged claim 7**

- 1        7. The invention as defined in claim 1 wherein said MOS transistor also has a
- 2        bulk terminal, said bulk terminal being connected to a second power supply terminal, and
- 3        wherein said power supply voltage supplied from said first power supply terminal is
- 4        lower than a voltage supplied from said second power supply terminal.

**Unchanged claim 8**

- 1        8. The invention as defined in claim 1 wherein said MOS transistor is a negative
- 2        metal oxide semiconductor (NMOS) transistor, said NMOS transistor also has a bulk
- 3        terminal, said bulk terminal being connected to a second power supply terminal, and
- 4        wherein said first power supply terminal is the positive power supply terminal for said
- 5        integrated circuit and said second power supply terminal is the negative power supply
- 6        terminal for said integrated circuit.

**Unchanged claim 9**

1       9. The invention as defined in claim 1 wherein said MOS transistor is a positive  
2 metal oxide semiconductor (PMOS) transistor, said PMOS transistor also has a bulk  
3 terminal, said bulk terminal being connected to a second power supply terminal, and  
4 wherein said first power supply terminal is the negative power supply terminal for said  
5 integrated circuit and said second power supply terminal is the positive power supply  
6 terminal for said integrated circuit.

**Unchanged claim 10**

1       10. The invention as defined in claim 1 wherein said voltage that is derived from  
2 said power supply voltage and has a larger absolute value than said power supply voltage  
3 supplied by said first power supply terminal and the same sign as said power supply  
4 voltage has a larger absolute value than said power supply by one threshold voltage of  
5 said MOS transistor.

**Unchanged claim 11**

1       11. The invention as defined in claim 1 wherein said voltage that is derived from  
2 said power supply voltage is generated from said power supply voltage by a high voltage  
3 generator.

**Unchanged claim 12**

1       12. The invention as defined in claim 1 further including on said integrated  
2 circuit a high voltage generator that generates said voltage that has a larger absolute value  
3 than said power supply voltage supplied by said first power supply terminal and the same  
4 sign as said power supply voltage.

**Unchanged claim 13**

1        13. The invention as defined in claim 1 further including on said integrated  
2        circuit a high voltage generator that generates said voltage that has a larger absolute value  
3        than said power supply voltage supplied by said first power supply terminal and the same  
4        sign as said power supply voltage, said high voltage generator comprising:  
5                an oscillator generating an oscillating output signal;  
6                a voltage doubler receiving as an input said oscillating output signal from said  
7        oscillator and supplying as an output a signal that has an average larger absolute value  
8        than said power supply voltage supplied by said first power supply terminal and the same  
9        sign as said power supply voltage;  
10               a clamp which receives as an input said output of said voltage doubler and  
11       supplies an output voltage substantially clamped to a prescribed value that has a larger  
12       absolute value than said power supply voltage supplied by said first power supply  
13       terminal and the same sign as said power supply voltage;  
14               and a ripple filter which filters said output of said clamp and supplies the output  
15       of said high voltage generator, which said voltage that has a larger absolute value than  
16       said power supply voltage supplied by said first power supply terminal and the same sign  
17       as said power supply voltage.

**Replacement claim 14**

1        14. (Amended) A circuit for use as an active inductor on an integrated circuit,  
2        comprising:  
3               a metal oxide semiconductor (MOS) transistor; and  
4               a beyond voltage generator which generates a beyond voltage that is either greater  
5        than the highest voltage or less than the lowest voltage being supplied to said integrated  
6        circuit by a power supply;  
7               wherein said MOS transistor is coupled to said beyond voltage generator so as to  
8        bias said MOS transistor with said beyond voltage and said MOS transistor is adapted to  
9        operate as said active inductor.

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**Replacement claim 15**

1        15. (Amended) The invention as defined in claim 14 wherein said beyond  
2        voltage generator comprises:  
3                an oscillator generating an oscillating output signal;  
4                a voltage doubler receiving as an input said oscillating output signal from said  
5        oscillator and supplying as an output a voltage signal that has an average voltage that is  
6        either greater than the highest voltage or less than the lowest voltage being supplied to  
7        said integrated circuit by a power supply;  
8                a clamp which receives as an input said output of said voltage doubler and  
9        supplies an output voltage substantially clamped to a prescribed value that is greater than  
10      the highest voltage or less than the lowest voltage being supplied to said integrated circuit  
11      by a power supply;  
12                and a ripple filter which filters said output of said clamp and supplies the output  
13      of said beyond voltage generator.

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**Replacement claim 16**

1        16. (Amended) An integrated circuit comprising a metal oxide semiconductor  
2        (MOS) transistor adapted to operate as an active inductor that is biased using a voltage  
3        generated on said integrated circuit that is outside the range of the voltage supplied by a  
4        power supply off of said integrated circuit for operating said integrated circuit.

**Unchanged claim 17**

1        17. The invention as defined in claim 16 wherein said MOS transistor is a  
2        negative metal oxide semiconductor (NMOS) transistor.

**Unchanged claim 18**

1        18. The invention as defined in claim 16 wherein said MOS transistor is a positive  
2        metal oxide semiconductor (PMOS) transistor.

**Unchanged claim 19**

1        19. The invention as defined in claim 16 wherein said active inductor is biased by  
2        coupling a gate of said MOS transistor to said voltage generated on said integrated circuit  
3        that is beyond the range of the voltage supplied by a power supply for operating said  
4        integrated circuit via an impedance.